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LIST OF MATERIALS CITED BY APPLICANT	INVENTOR'S NAME: Jared LeVan ZERBE et al.	EXAMINER: Unassigned
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U.S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS AND SUBCLASS	TRANSLATION PROVIDED	
						Yes	No

		OTHER MATERIALS (Including Author, Title, Date, Pertinent Pages, Etc.)
SL	1.	M. RAU et al., "Clock/Data Recovery PLL Using Half-Frequency Clock," IEEE Journal Of Solid-State Circuits, Vol. 32, No. 7, July 1997, pp. 1156-1159
SL	2.	CHIH-KONG et al., "A 0.8-μm CMOS 2.5 Gb/s Oversampling Receiver and Transmitter for Serial Link," IEEE Journal Of Solid-State Circuits, Vol. 31, No. 12 December 1996, pp. 2015-2023
SL	3.	RAMIN FARJAD-RAD et al., "A 0.3-μm CMOS 8-Gb/s 4-PAM Serial Link Transceiver," IEEE Journal Of Solid-State Circuits, Vol. 35, No. 5, May 2000, pp. 757-764
SL	4.	KUN-YUNG KEN CHANG et al., "A 0.4-4Gb/s CMOS Quad Transceiver Cell using On-chip Regulated Dual-Loop PLLs," 4 pages

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